Remarks

Claims 1-4, 6-26, and 28-31 are pending in the current application. No claims have been amended.

Indication of Allowable Subject Matter

Claims 4, 7-10, 15-19, 21-23, 29 and 30 stand objected to as being dependent upon a rejected base claim, but are indicated as allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicants thank the Examiner for the indication of allowable subject matter.

35 U.S.C. 102 Rejections

Claims 1-3 and 6, 11-12, 14, 24-26, 28 and 31 have been rejected under 35 U.S.C. 102(b) as being anticipated by Naganawa, U.S. Pat. No. 6,219,280.

Claim 20 has been rejected under 35 U.S.C. 102(e) as being anticipated by Santin, U.S. Pat. No. 6,847,574.

Applicant respectfully traverses these rejections because the cited references do not disclose or suggest every element of any claim, as the following analysis shows.

CLAIM 1

Regarding Claim 1, Naganawa at least fails to teach "wherein the detecting is performed during an erase operation" as recited in amended Claim 1.

The Office Action dated 11/15/05 asserts that "the detecting is performed during an erase operation [erase – verify – s200]" with reference to Figure 4 and column 10 of Naganawa. However, s200 of Naganawa refers to "Erase Verify Processing" which includes multiple separate operations, as illustrated in Figure 6 of Naganawa. In particular, Naganawa discloses an erase operation s202 separate from an erase verify operation s204.

> "[D]ata of all memory cells 1 which are to be erased are simultaneously erased (S202). The simultaneous erase processing itself is the same as a conventional one, and performed by applying a predetermined voltage between the floating gates and semiconductor substrates of all memory cells to be erased. Then, the tester supplies a start address signal to the address controller 3, and sets the start address in the internal address generation circuit 13 (S203). ... The verify circuit 7 compares the threshold level of the memory cell with a predetermined verify threshold level to verify whether a proper erase is done (S204)." See Column 7, line 64 through Column 8, line 20:

Accordingly, for at least the foregoing reasons, Naganawa fails to teach the limitations of Claim 1. The rejection of Claim 1 is thus unsupported, and must be withdrawn. Claims 2-3 and 6, 11-12 depend from allowable Claim 1 and are allowable for at least this reason.

CLAIM 14

Regarding amended Claim 14, Naganawa at least fails to teach a failure detection unit "to monitor electrical characteristics in the plurality of accessible memory units during an erase operation" as recited in Claim 14.

As illustrated above with respect to Claim 1, Naganawa discloses an erase operation s202 separate from an erase verify operation s204. Thus, Naganawa does not

teach a failure detection unit configured to monitor electrical characteristics during an erase operation.

Accordingly, for at least the foregoing reasons, Naganawa fails to teach the limitations of Claim 14. The rejection of Claim 14 is thus unsupported, and must be withdrawn.

CLAIM 20

Regarding Claim 20, Santin at least fails to teach "a failure detection unit coupled to the plurality of accessible memory units configured to monitor electrical characteristics in the plurality of accessible memory units and to detect a electrical characteristic that identifies a defect in one of the plurality of accessible memory units" as recited in Claim 20.

The Office Action dated 11/15/05 asserts that Santin discloses such a failure detection unit with reference to a redundancy circuit 108 and refers to column 1, lines 25-40. Here, Santin discloses redundancy circuits that detect whether defective memory cells exist, configure memory devices to avoid the defective memory cells, and redirect memory accesses from the defective memory cells to the nondefective memory cells. Santin does not disclose how the redundancy circuits detect defective memory cells. Thus, Santin does not teach a failure detection unit configured to monitor electrical characteristics in the plurality of accessible memory units.

Accordingly, for at least the foregoing reasons, Santin fails to teach the limitations of Claim 20. The rejection of Claim 20 is thus unsupported, and must be withdrawn. Claims 21-23 depend from allowable Claim 20 and are allowable for at least this reason.

CLAIM 24

For similar reasons as argued with respect to Claim 1 above, with respect to amended Claim 24, Naganawa at least fails to teach "wherein the electrical characteristic is detected during an erase operation" as recited in Claim 24.

Accordingly, for at least the foregoing reasons, Naganawa fails to teach the limitations of Claim 24. The rejection of Claim 24 is thus unsupported, and must be withdrawn. Claims 25-26 and 28-31 depend from allowable Claim 24 and are allowable for at least this reason.

35 U.S.C. 103 Rejections

Claim 13 has been rejected under 35 U.S.C. 103(a) as being unpatentable over Naganawa in view of Gudesen et al., U.S. Pat. No. 6,380,597. Claim 13 depends from allowable Claim 13 and is allowable for at least this reason.

Conclusion

For the foregoing reasons, it is submitted that the application is in condition for allowance, and indication of allowance by the Examiner is respectfully requested. If the Examiner has any questions concerning this application, he or she is requested to telephone the undersigned at the telephone number shown below as soon as possible. If any fee insufficiency or overpayment is found, please charge any insufficiency or credit any overpayment to Deposit Account No. 02-2666.

Respectfully submitted,

Intel Corporation

Date: February 14, 2006 /Rita M. Wisor/

Rita M. Wisor
Reg. No. 41,382

Attorney Phone Number: (512) 732-3923

Correspondence Address: Blakely Sokoloff Taylor & Zafman, LLP
12400 Wilshire Blvd
Seventh Floor
Los Angeles, California 90025-1026